FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT



Applicant(s): W. Rhee et al.
Docket No.: YOR920030258US1
Serial No.: 10/697,751
Filing Date: October 30, 2003
Group: 2816

## U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NO. | DATE | NAME | CLASS/SUBCLASS | FILING DATE IF APPROPRIATE |
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## FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NO. | DATE | COUNTRY | CLASS/SUBCLASS | TRANSLATION YES | TRANSLATION NO |
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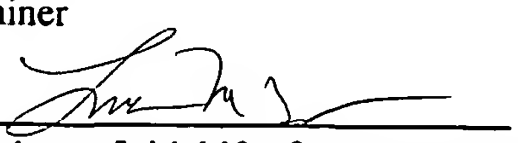
## OTHER DOCUMENTS

| EXAMINER INITIAL | REF NO. | AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC. |
|---|---|---|
| LR | 1. | S. Lee et al., "A 5 Gb/s 0.25 μm CMOS Jitter-Tolerant Variable-Interval Oversampling Clock/Data Recovery Circuit," ISSCC, Session 15, Gigabit Communications, pp. 463-465, February 2002. |
| LR | 2. | J. Savoj et al., "A 10-Gb/s CMOS Clock and Data Recovery Circuit with a Half-Rate Linear Phase Detector," IEEE Journal of Solid-State Circuits, Vol. 36, No. 5, pp. 761-767, May 2001. |
| LR | 3. | W. Rhee, "A Low Power, Wide Linear-Range CMOS Voltage-Controlled Oscillator," Proc. of IEEE, pp. II-85-II-88, May 1998. |

Examiner 

Date Considered 6/29/2004

**Examiner:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.